Reliability evaluation for

MDmesh™ DM2 Technology 8" Wafer Front-end Capacity Extension - Ang Mo Kio (Singapore) - INDUSTRIAL

Process change

General Information	
Commercial Product	:STB43N60DM2 STD13N60DM2 STW63N65DM2
Silicon Line	: FQ6L – FQ63 – FQF9
Product Description	*:* Power MOSFET
Package	: D²PAK – DPAK - TO-247
Silicon Technology	: MDmesh™ DM2
Division	*:Power Transistor Division*

Traceability	
Diffusion Plant	: SG8" (Singapore)
Assembly Plant	: ST Shenzhen (China)
Reliability Lab	: Catania (Italy)

Reliability Assessment	
Passed	☒

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	13 February 2019	A.SETTINIERI	FINAL REPORT

APPROVED BY:
Corrado CAPPELLO
ADG Q&R department - Catania
STMicroelectronics

TABLE OF CONTENTS

1. RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Reliability evaluation MDmesh™ DM2 Technology 8" Wafer Front-end Capacity Extension - Ang Mo Kio (Singapore) - INDUSTRIAL

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with JESD47 and 0061692 internal spec Guidelines and are listed in the Test Plan.
For details on test conditions, generic data used and spec reference see test results summary at Par.3 .

#	Stress	Abrv	Reference	Test Flag	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	Y	
2	External Visual	EV	JESD22B-101	Y	
3	High Temperature Storage Life	HTSL	JESD22B-101	Y	
4	High Temperature Gate Bias	HTGB	JESD22A-108	Y	
5	High Temperature Reverse Bias	HTRB	JESD22A-108	Y	
6	Pre-conditioning	PC	JESD22A-113	Y	
7	Temperature Cycling	TC	JESD22A-104	Y	
8	Autoclave	AC	JESD22A-102	Y	
9	High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	Y	
10	Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	Y	
11	ESD Characterization	ESD (HBM, CDM)	ESDA-JEDEC JES-001 and AINSI-ESD S5.3.1	Y	

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die and package oriented test showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.
ESD is accordance with ST spec.

On the basis of the overall results obtained, we can give a positive judgment on the reliability evaluation for MDmesh™ DM2 Technology 8" Wafer Front-end Capacity Extension for Industrial product diffused in SG8" (Singapore) Fab and assembled in ST Shenzhen (China).
In agreement with JESD47 and 0061692 internal spec.

2. DEVICE/TEST VEHICLE CHARACTERISTICS

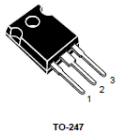
2.1 Generalities

Power MOSFET MDmesh™ DM2

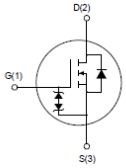
2.2 Pin Connection

D²PAK

DPAK



TO-247



2.3 Traceability

Reference "Product Baseline" document if existing, else provide following chapters/information:

D.U.T.: STB43N60DM2 **PACKAGE: D²PAK**

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	6840 x 5050 µm²
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package code description	D²PAK
Lead frame/Substrate	FRAME TO263 Dt 40u Ve5 OpD/G/H Selected Ni/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate: Al/Mg 5 mils - Source: Al 10mils
Molding compound	Halogen Free

D.U.T.: STD13N60DM2 PACKAGE: DPAK

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	TEOS+Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	3980 x 2900 µm^2
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package code description	DPAK
Lead frame/Substrate	FRAME TO251 3L Big Ve5 OpE 30u Selected Ni/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate: Al/Mg 5 mils - Source: Al 10mils
Molding compound	Halogen Free

D.U.T.: STW63N65DM2 PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	TEOS + Nitride
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10390 x 6850 µm^2
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	ST Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO-247 3L Selected Ni/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate: Al/Mg 5 mils - Source: Al 10mils
Molding compound	Halogen Free

Reliability Testing Information	
Reliability laboratory location	Catania (Italy)
Electrical testing location	Catania (Italy)

3. TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Commercial Product	Silicon Line	Package	Wafer Fab	Assembly plant	Note
1	STB43N60DM2	FQ6L	D²PAK	SG8" (Singapore)	ST Shenzhen (China)	
2	STD13N60DM2	FQ63	DPAK			
3	STW63N65DM2	FQF9	TO-247			

3.2 Test results summary

Test	Std ref.	Conditions	SS	Steps	Failure/SS		
					Lot 1	Lot 2	Lot 3
TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.			235	235	235
External visual	JESD22 B-101	All devices submitted for testing			235	235	235
Silicon oriented tests							
HTSL	JESD22B 101	TA = 150°C	135	1000 h	0/45	0/45	0/45
HTRB	JESD22 A-108	Tj = 150°C, BIAS = 520V	45	1000 h			0/45
		Tj = 150°C, BIAS = 480V	90		0/45	0/45	
HTGB	JESD22 A-108	Tj = 150°C, BIAS = 30V	135	1000 h	0/45	0/45	0/45
Package oriented Tests							
Pre - conditioning	JESD22A 113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=245°C 3 times	All SMD devices to be subjected to H3TRB, TC, AC, IOL	Final	Pass		
		Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times				Pass	
TC	JESD22 A-104	TA=-55°C TO 150°C	75	1000cy	0/25	0/25	0/25
AC	JESD22 A-102	TA=121°C ; PA=2ATM	75	96h	0/25	0/25	0/25
H3TRB	JESD22 A-101	TA=85°C ; RH=85% BIAS= 100V	75	1000 h	0/25	0/25	0/25
IOL	MIL-STD-750 Method 1037	ΔTj ≥100°C	75	15Kcy	0/25	0/25	0/25
ESD	ESDA–JEDEC JES–001 ANSI – ESD S5.3.1	CDM / HBM	9		0/3 0/3	0/3 0/3	0/3 0/3

Catania, February 14 2019

Automotive Discrete Group (ADG)
Power Transistor Division
HV Business Unit
Process Change Notification

MDmesh™ DM2 Technology Power MOSFET Transistors 8" Wafer Front-end Capacity Extension Ang Mo Kio INDUSTRIAL

Dear Customer,

Following the continuous improvement of our service and in order to increase Front-end Capacity, this document is announcing the new 8" wafer line for MDmesh™ DM2 Technology of Power MOSFET Transistors in ST's Ang Mo Kio (Singapore) FAB.

MDmesh™ DM2 Technology manufactured in 8" wafer size of Ang Mo Kio (Singapore) FAB, guarantees the same quality and electrical characteristics as per current production. This production is already born with front top metal AlCu+Ti/TiN barrier as per PCN ADG/18/11269 dated December 16 2018.

The involved product series are listed in the table below:

Product Family	Technology	Part Number
Power MOSFET Transistors	MDmesh™ DM2	STxxxN6xDM2xx

Any other Product related to the above series, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 08-2019.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistors	D^2PAK DPAK TO-247	STB43N60DM2 STD13N60DM2 STW63N65DM2

Change implementation schedule:

The production start and first shipments will be implemented after week 20 of 2019.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of 8" wafer size, manufactured in ST's Ang Mo Kio (Singapore) FAB, will be ensured by internal code (Finished Good) and Q.A. number.

Yours faithfully.